GW1N/GW1NR series of FPGA Products Schematic Manual

Introduction

You should follow a series of rules for circuit board design when using the GW1N/GW1NR series of FPGA products. This manual describes the characteristics and special features of the GW1N/GW1NR series of FPGA products and provides a comprehensive checklist to guide design processes. The main contents of this guide are as follows:

- Power Supply
- JTAG Download
- MSPI Download
- Clock Pin
- Differential Pin
- READY, RECONFIG_N, DONE
- MODE
- JTAGSEL_N
- FASTRD_N
- Dual-purpose Pin
- FPGA External Crystal Oscillator Circuit Reference
- Bank Voltage
- Configuration Modes Supported by Each Device
- Pinout

Power Supply

Overview

The GW1N/GW1NR series of FPGA products support lower voltage (LV) and upper voltage (UV) with low power, instant on, and non-volatile power features. LV supports 1.2V core voltages. UV supports 1.8V, 2.5V, and 3.3V core voltages, and has a built-in linear voltage regulator. LV and UV have the same functions, and the pins are compatible.

Voltage types include core voltage (VCC), auxiliary voltage (VCCX) and bank voltage (VCCIO).

VCCX is an auxiliary power supply that is used to connect the internal part of the chip, with a 2.5V or 3.3V power supply. If no VCCX exists, I/O, OSC, and BSRAM circuits will be impacted and the chip will not be functional.

Power DC Voltage Requirement

GW1N(R) series devices have several different power rails, VCC, VCCX and some VCCIOs. In order to release the Power On Reset, VCC, VCCX and some special VCCIOs have to be powered. Please refer to Table 4-1 "Power Rails Monitored by POR Circuits of Different Devices" in Chapter 4.1 Power-up Sequence of *UG290, Gowin FPGA Products Programming and Configuration Guide* for required VCCIO rails of different devices. Vccx should be always no less than VCCIO, or there will be some unexpected leakage on VCCIO.

For the recommended operating range for each power voltage, refer to the "Power" sheet in the following pinouts.

- UG107, GW1N-1 Pinout
- UG167, GW1N-1S Pinout
- UG174, GW1N-1P5 Pinout
- UG171, GW1N-2 Pinout
- UG105, GW1N-4 Pinout
- UG114, GW1N-9 Pinout
- UG804, GW1NR-1 Pinout
- UG805, GW1NR-2 Pinout
- UG116, GW1NR-4 Pinout
- UG803, GW1NR-9 Pinout

Power Sequence

Theoretically the devices can be powered up and powered down by any sequence. But during the power ramping procedure, if VCCX is lower than VCCIO, VCCIO could have high current (hundreds of mA). This high current could maintain until VCCX is no less than VCCIO. To prevent this unexpected current, we recommend power on VCCX before/with VCCIOs.

No special power sequence requirement for VCC.

Recommended Reference Range of Power-up Time

Recommended reference range of power-on time for VCC is 0.2ms~2ms. And the power supply ramping rate of VCCIO and VCCX is as shown in “Power Supply Ramp Rate” table in Chapter 4.1.3 “Power Supply Ramp Rate” of *DS100, GW1N series of FPGA Products Data Sheet*. You can ignore the reference range of power-on time and recommendations in the “Power Supply Ramp Rate” table mentioned above (except VCCIO) if you can meet the following calculation method in Power Supply Ramping Rate.

Note!

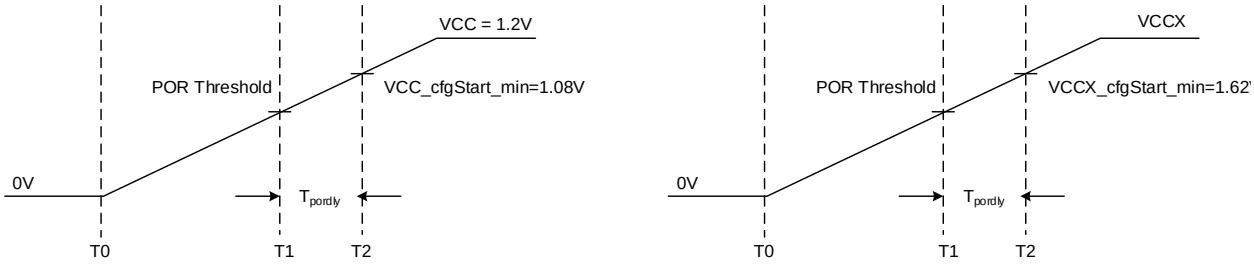
- If the power-on time is more than 2ms, you need to ensure that the power-on in sequence is VCC, and then VCCX/VCCIO; Or you need to calculate the safe ramping time by the following formula in Power Supply Ramping Rate.
- If the power-on time is less than 0.2ms, it is recommended to increase the capacitance to prolong the power-on time.

Power Supply Ramping Rate

For GW1N devices, after the POR is released, the config logic will access the internal flash to read out the manufacture data for initializing. To make sure the internal flash is ready before this read operation, we have power ramping rate requirement.

The internal flash is powered by V_{CC} and V_{CCX}. As in the flash spec, VCC≥1.08V & VCCX≥1.62V is required for the reading operation. The system power rails have to meet this condition when the device starts to initializing.

Figure 1 Power Ramping Waveform



POR threshold voltage of VCC and VCCX is as shown in Table 4-5 “POR Voltage” in Chapter 4.1.5 “POR Feature” of *DS100, GW1N series of FPGA Products Data Sheet*. POR delay time: $T_{pordly\text{-}min}$=500us,

$T_{pordly\text{-}typ}$=750us, $T_{pordly\text{-}max}$=1ms.

To calculate the ramping time requirement, first we need to know which power rail will achieve the POR trip point at last. This is T1, when system POR will be released. Then we can get T2 which equals to T1 + T_{pordly}, when the device starts to access the internal flash. We need to guarantee VCC≥1.08V & VCCX≥1.62V at T2.

Take GW1N-4 as an example, assuming VCC is powered on at last and VCCX and VCCIOs are stable before VCC, the POR release time will depend on VCC rail. If the ramping time is 3.3ms, VCC POR threshold is around 0.9V of GW1N-4 per Table 4-5 “POR Voltage” in Chapter 4.1.5 “POR Feature” of *DS100, GW1N series of FPGA Products Data Sheet*.

T1 = 3.3ms * 0.9V/1.2V = 2.475ms

T2 = T1 + $T_{pordly\text{-}min}$ = 2.975ms,

Thus, we can get $VCC_{cfgstart}$ = 1.2V * 2.975ms/3.3ms = 1.08V bigger than minimum=1.08V requirement. Then it is a safe ramping rate.

Note!

The above calculation is based on the fact that the power supply is linearly lifted.

If VCCX is the last rail powered on. We have to make sure it meets the $VCCX_{cfgstart\_min}$ =1.62V requirement.

For UV devices, please use 0.3V voltage drop of the internal LDO to calculate the VCC ramping time requirement, i.e. at T2, the minimum voltage should be 1.08 + 0.3 = 1.38V.

Total Power

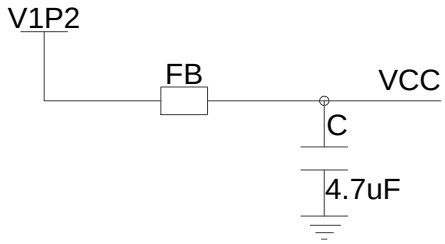
For specific density, packages, and resource utilization, GPA tools can be used to evaluate and analyze the power consumption.

Power Filter

Each FPGA power input pin is connected to the ground with a 0.1uF ceramic capacitor.

The input end of the VCC core voltage should primarily conduct the noise processing. Specific reference is as shown in Figure 2.

Figure 2 V_{CC} Noise processing on the Input End of the Vcc Core Voltage



FB is a ferrite bead, reference model mh2029-221y, ceramic capacitance 4.7uF. It offers an accuracy of more than ±10%.

JTAG Download

Overview

JTAG download is used for downloading the bitstream data into the SRAM, on-chip Flash or off-chip Flash of the FPGA.

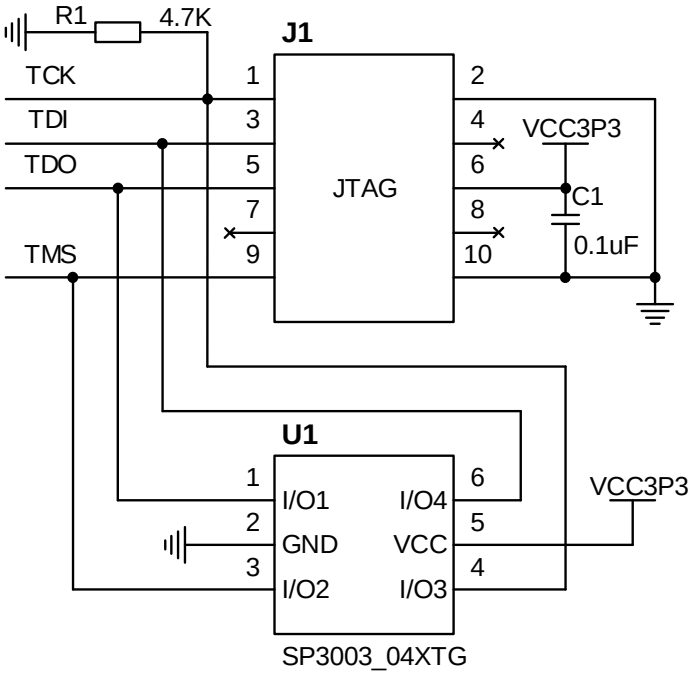
Signal Definition

Table 1 Signal Definition of JTAG Configuration Mode

Name	I/O	Description
TCK	I	Serial clock input in JTAG mode
TMS	I, internal weak pull-up	Serial mode input in JTAG mode
TDI	I, internal weak pull-up	Serial data input in JTAG mode
TDO	O	Serial data output in JTAG mode

JTAG Circuit Reference

Figure 3 JTAG Circuit Reference



Note!

- The resistance accuracy is not less than 5%;
- The power supply of the 6th pin in the JTAG socket can be adjusted to VCC1P2, VCC1P5, VCC1P8 and VCC2P5 as required.
- It is recommended to add ESD protection chip on JTAG signal for better protection of JTAG pins from electrostatic damage, optional model: SP3003_04XTG.

MSPI Download

Overview

As a master device, the MSPI configuration mode reads the configuration data automatically from the off-chip Flash and sends it to the FPGA SRAM.

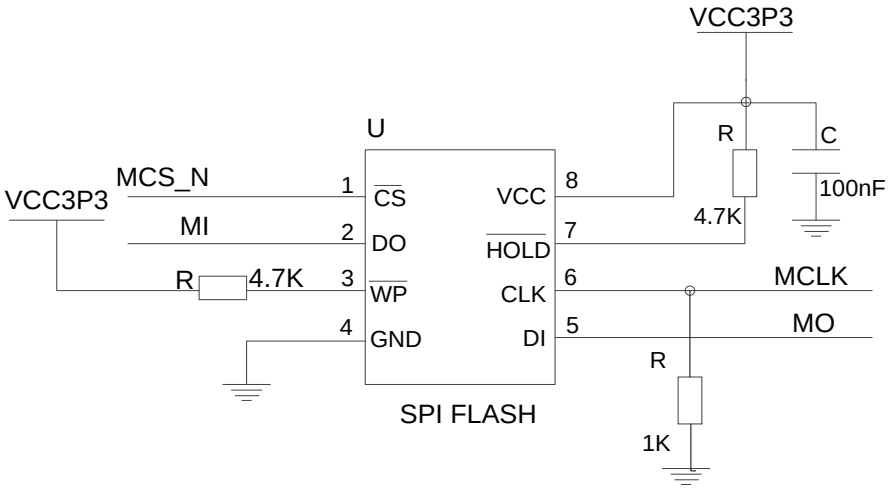
Signal Definition

Table 2 Signal Definition for MSPI Configuration Mode

Name	I/O	Description
MCLK	O	Clock output in MSPI mode
MCS_N	O	MCS_N in MSPI mode, low-active
MI	I	Data input in MSPI mode
MO	O	Data output in MSPI mode

MSPI Circuit Reference

Figure 4 MSPI Circuit Reference



Note!

- 1K pull-down resistance is required for MCLK signal.
- The resistance accuracy is not less than 5%.

Clock Pin

Overview

The clock pins include GCLK global clock pins and PLL clock pins.

- GCLK: The GCLK pins in the GW1N/GW1NR series of FPGA products distribute in the L and R quadrants. Each quadrant provides eight GCLK networks. The optional clock resources of the GCLK can be I/Os or CRU. Selecting the clock from the dedicated I/Os can result in better timing.
- PLL: Frequency (multiply and division), phase, and duty cycle can be adjusted by configuring the parameters.

Signal Definition

Table 3 Signal Definition for Clock Pin

Name	I/O	Description
GCLKT_[x]	I/O	Pins for global clock input, T(True), [x]: global clock No.
GCLKC_[x]	I/O	Pins for Global clock input, C(Comp), [x]: global clock No.
LPLL_T_fb/RPLL_T_fb	I	L/R PLL feedback the input pin, T(True)
LPLL_C_fb/RPLL_C_fb	I	L/R PLL feedback the input pin, C(Comp)
LPLL_T_in/RPLL_T_in	I	L/R PLL clock input pin, T(True)
LPLL_C_in/RPLL_C_in	I	L/R PLL clock input pin, C(Comp)

Clock Input Selection

If the external clock inputs as a PLL clock, the user is advised to input from the PLL dedicated pin. And the PLL_T end is selected if the external clock inputs from the single-end.

GCLK is the global clock and is directly connected to all resources in the device. The GCLK_T end is advised if the GCLK inputs from the single-end.

Differential Pin

Overview

Differential transmission is a form of signal transmission technology that operates according to differences between the signal line and the ground line. The differential transmit signals on these two lines, the amplitude of the two signals are equal and have the same phase but demonstrate opposite polarity.

LVDS

LVDS is a low-voltage differential signal that offers low power consumption, low bit error rate, low crosstalk, and low radiation. It facilitates the transmission of data using a low-voltage swing high-speed differential. Different packages employ different signals. Please refer to the True LVDS section of the Package Pinout Manual for further details.

Note!

- Differential input requires an external 100 ohms termination resistor.
- The differential line impedance of PCB is controlled at about 100 ohms.

READY, RECONFIG_N, DONE

Overview

RECONFIG_N is a reset function within the FPGA programming configuration. FPGA can't configure if RECONFIG_N is low.

As a configuration pin, a low level signal with pulse width no less than 25ns is required to start GowinCONFIG to reload bitstream data according to the MODE setting value. You can control the pin via the write logic and trigger the device to reconfigure.

READY, the FPGA can configure only when the READY signal is high. The device should be restored by using the power on or triggering RECONFIG_N when the READY signal is low.

As an output configuration pin, FPGA can be indicated for the current configuration state. If the device meets the configuration condition, READY signal is high. If the device fails to configure, the READY signal changes to low. As an input configuration pin, you can reduce the READY signal via its own logic or manually operate outside the device to delay configuration.

DONE, the DONE signal indicates that the FPGA is configured successfully. The signal is high after successful configuration.

As an output configuration pin, FPGA can be indicated whether the current configuration is successful. If configured successfully, DONE is high, and the device enters into a working state. If the device failed to configure, the DONE signal remains low. For the input type, the user can reduce the READY signal via its own internal logic or manually operate outside the device to delay progression to user mode.

When the RECONFIG_N or READY signals are low, the DONE signal

is low. DONE has no influence when SRAM is configuried through the JTAG circuit.

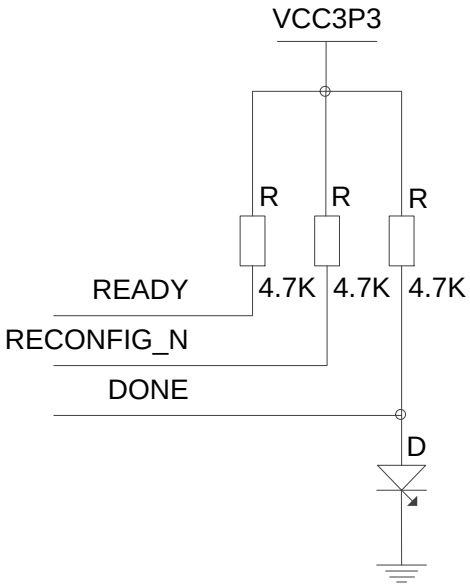
Signal Definition

Table 4 READY, RECONFIG_N, DONE Signal Definition

Name	I/O	Description
RECONFIG_N	I, internal weak pull-up	Low level pulse: start new GowinCONFIG configuration
READY	I/O	High-level pulse: The device can currently be programmed and configured;
		Low-level pulse: The device cannot be programmed and configured,
DONE	I/O	High-level pulse: The device has been successfully programmed and configured;
		Low-level pulse: The configuration is incomplete or has failed.

READY, RECONFIG_N, DONE Reference Circuit

Figure 5 READY, RECONFIG_N, DONE Reference Circuit



Note!

- The upper pull power supply is the bank voltage value of the corresponding pin;
- The resistance accuracy is not less than ± 5%.

MODE

Overview

MODE spans the MODE0, MODE1, MODE2, and GowinCONFIG configuration modes. When the FPGA powers on or a low pulse triggers the RECONFIG_N mode, the device enters the corresponding GowinCONFIG state according to the MODE value. MODE [2:0] is used to select the GowinCONFIG programming configuration mode. The configuration mode can be fixed by using pull-up or pull-down resistors. It is recommended to use a 4.7K resistor for pull-up or a 1K resistor for pull-down. As the number of pins for each package is different, some MODE pins are not all packaged, and the unpacked MODE pins are grounded or internally connected to the power supply inside the devicce. Please refer to the corresponding PINOUT manual for further details.

Signal Definition

Table 5 MODE Signal Definition

Name	I/O	Description
MODE2	I, internal weak pull-up	GowinCONFIG modes selection pin.
MODE1	I, internal weak pull-up	GowinCONFIG modes selection pin.
MODE0	I, internal weak pull-up	GowinCONFIG modes selection pin.

Mode Selection

Table 6 Mode Selection

Configuration Modes		MODE[2:0][1]	Description
JTAG		XXX[2]	The LittleBee® Family of FPGA products are configured via JTAG interface by external Host.
GowinCONFIG	AUTO BOOT	000	FPGA reads data from embedded Flash for configuration
	I2C[6]	100	FPGA products are configured via I2C interface by external Host.
	SSPI[3]	001	FPGA products of LittleBee® Family are configured via SPI interface.
	MSPI[3]	010	As a Master, FPGA reads data from external Flash (or other devices) via the SPI interface[3].
	DUAL BOOT[4]	110	FPGA reads data from external Flash first and if the external Flash configuration fails, it reads from the Internal Flash.
	SERIAL[5]	101	External Host configures FPGA products of LittleBee® Family via DIN interface.
	CPU[5]	111	External Host configures FPGA products of LittleBee® Family via DBUS interface.

Note!

- [1] The unbound mode pins are grounded or internally connected to the power supply by default.
- [2] The JTAG configuration mode is independent of MODE value.
- [3] The SPI interfaces of the SSPI and MSPI modes are independent of each other.
- [4] Currently GW1N(R)-4/GW1N(R)-4B do not support DUAL BOOT.
- [5] The CPU configuration mode and SERIAL configuration mode share SCLK, WE_N and CLKHOLD_N. The data bus pins for the CPU configuration mode share pins with MSPI and SSPI configuration modes.
- [6] I2C is only supported in some devices.

JTAGSEL_N

Overview

Select the signal in JTAG mode. If the JTAG pin is set as GPIO in Gowin software, the JTAG pin is changed to GPIO pin after being powered on and successfully configured. The JTAG pin can be recovered by reducing the JTAGSEL_N. The JTAG configuration functions are always available if no JTAG pin multiplexing is set.

Signal Definition

Table 7 JTAGSEL_N Signal Definition

Pin Name	I/O	Description
JTAGSEL_N	I, internal weak pull-up	Restore JTAG pin from GPIO to configuration pin. Low level is valid

Note!

As GPIO, the JTAGSEL_N pin and four pins (TCK, TMS, TDI, and TDO) configured with JTAG are incompatible: the JTAG pin can only be used as a configuration pin if JTAGSEL_N is set as GPIO. JTAGSEL_N can only be used as a configuration pin if JTAG is set as GPIO.

FASTRD_N

Overview

In MSPI configuration mode, signals are selected via reading the SPI flash speed rate. FASTRD_N is normal read mode if it is high level; FASTRD_N is high speed read mode if it is low level. Each manufacturer's Flash high speed read instruction is different; please refer to the corresponding Flash data manual.

Signal Definition

Table 8 FASTRD_N Signal Definition

Pin Name	I/O	Description
FASTRD_N	I/O	● As a configuration pin: Input, internal weak pull up, sample MSPI configuration value at READY signal rising edge; ● As a GPIO: Input or putput.

Note!

- High-level: Normal Flash access mode, the clock frequency should be less than 30MHz;
- Low-level: High-speed Flash access mode, the clock frequency is greater than 30MHz and less than 80MHz.

Dual-purpose Pin

Overview

Configure pin multiplexing refers to configuring during power-on, which is used as a normal I/O after downloading the bitstream file.

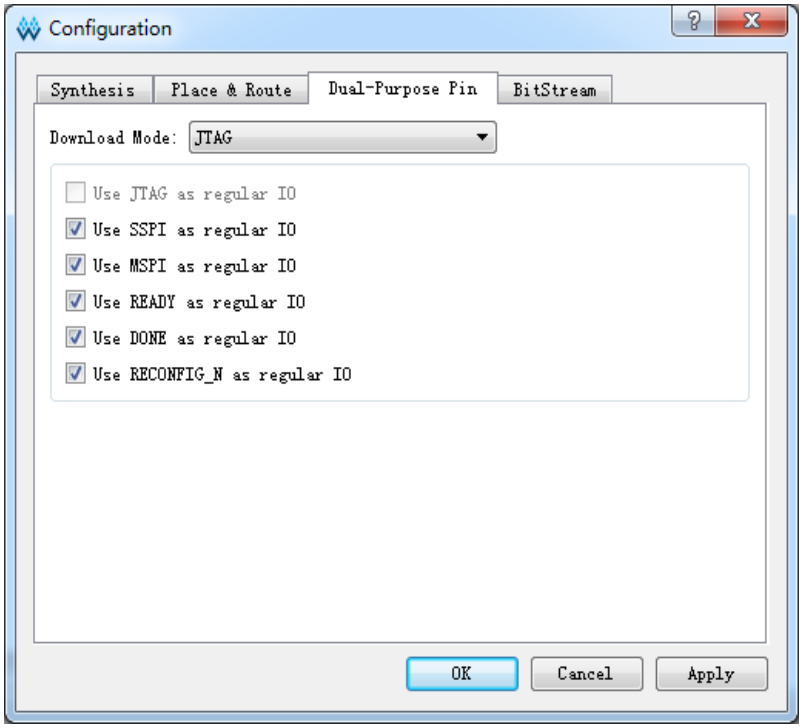
Configure pin multiplex via the Gowin Software:

a). Open the corresponding project in Gowin Software;

b). Select "Project > Configuration > Dual-Purpose Pin" from the menu options, as shown in Figure 6;

c). Check the corresponding option to set the pin multiplex.

Figure 6 Dual-purpose Pin



Dual-purpose Pin

- SSPI: As a GPIO, SSPI can be used as input or output type;
- MSPI: As a GPIO, MSPI can be used as input or output type;
- RECONFIG_N GPIO can only be used as an output type. For smooth configuration, set the initial value of RECONFIG_N as high when multiplexing it.
- READY: As a GPIO, READY can be used as an input or output. As an input GPIO for READY, the initial value of READY should be 1 before

configuring. Otherwise, the FPGA will fail to configure;

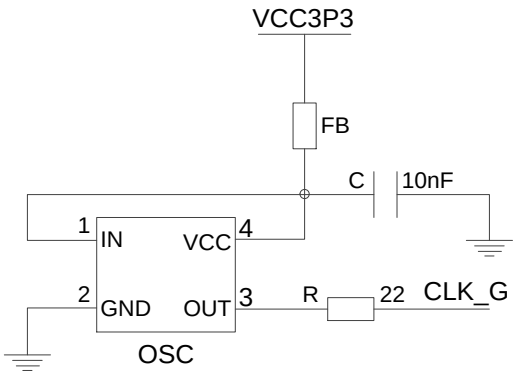
- DONE: As a GPIO, DONE can be used as an input or output type. If DONE is used as an input GPIO, the initial value of DONE should be 1 before configuring. Otherwise, the FPGA will fail to enter the user mode after configuring;
- JTAG: As a GPIO, JTAG can be used as an input or output type;
- JTAGSEL_N: As a GPIO, JTAGSEL_N can be used as an input or output type.
- DONE: as a GPIO, DONE can be used as an input or output type. In order to smoothly configure, the user multiplexes the MODE pin, the correct configuration mode value is needed to provided during configuration (power-on or low-level pulse triggers RECONFIG_N). Three pins can be multiplexed in the MODE. Unpackaged devices are grounded or connected to the power supply internally. Please refer to PINOUT manual of the corresponding device for details. For the MODE value corresponding to different configuration modes, please refer to the corresponding device configuration and programming manual

Note!

If the Number of I/O port is sufficient, use non-multiplexed pins first.

FPGA External Crystal Oscillator Circuit Reference

Figure 7 FPGA External Crystal Oscillator Circuit Reference



FB is a magnetic bead, with MH2029-221Y reference model, more than ±5% resistance accuracy, and more than ±10% capacitance accuracy.

Bank Voltage

For the detailed Bank voltage requirements, please refer to the following manuals.

- UG107, GW1N-1 Pinout
- UG105, GW1N-4 Pinout
- UG171, GW1N-2 Pinout

- UG174, GW1N-1P5 Pinout
- UG114, GW1N-9 Pinout
- UG167, GW1N-1S Pinout
- UG116, GW1NR-4 Pinout
- UG803, GW1NR-9 Pinout
- UG804, GW1NR-1 Pinout
- UG805, GW1NR-2 Pinout

Configuration Modes Supported by Each Device

GW1N-1

Table 9 GW1N-1 Configuration Modes

Package	JTAG	AUTO BOOT	SSPI	MSPI	DUAL BOOT	SERIAL	CPU
CS30	Yes	Yes	Yes	No	No	No	No
QN32	Yes	Yes	Yes	No	No	No	No
QN48	Yes	Yes	Yes	Yes	No	No	No
LQ100	Yes	Yes	Yes	No	No	No	No
LQ144	Yes	Yes	Yes	Yes	No	No	No

GW1N-1S

Table 10 GW1N-1S Configuration Modes

Package	JTAG	AUTO BOOT	SSPI	MSPI	DUAL BOOT	SERIAL	CPU
FN32	Yes	Yes	No	No	No	No	No
CS30	Yes	Yes	No	No	No	No	No

GW1N-2

Table 11 GW1N-2 Configuration Modes

Package	JTAG	AUTO BOOT	I^2C	SSPI	MSPI	DUAL BOOT	SERIAL	CPU
CS42	Yes	Yes	No	No	No	No	No	No
CS42H[1]	Yes	Yes	Yes	No	No	No	No	No
LQ100	Yes	Yes	No	No	No	No	No	No
LQ144	Yes	Yes	No	No	No	No	No	No
MG121	Yes	Yes	No	No	No	No	No	No
MG132	Yes	Yes	No	No	No	No	No	No
LQ100X[1]	Yes	Yes	Yes	No	No	No	No	No
LQ144X[1]	Yes	Yes	Yes	No	No	No	No	No
MG121X[1]	Yes	Yes	Yes	No	No	No	No	No
MG132X[1]	Yes	Yes	Yes	No	No	No	No	No
MG49[1]	Yes	Yes	Yes	No	No	No	No	No
QN48	Yes	Yes	No	Yes	No	No	No	No

Package	JTAG	AUTO BOOT	I²C	SSPI	MSPI	DUAL BOOT	SERIAL	CPU
QN48H	Yes	Yes	No	Yes	No	No	No	No
MG132H[1]	Yes	Yes	Yes	Yes	No	No	No	No
QN32X[1]	Yes	Yes	Yes	No	No	No	No	No
QN88	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No
QN32	Yes	Yes	No	No	No	No	No	No
CS100H[1]	Yes	Yes	Yes	Yes	No	No	No	No
LQ144F	Yes	Yes	No	No	No	No	No	No

Note!

[1] When I²C is supported, the SDA and SCL pins need to be externally pulled up; when AUTOBOOT is supported, the SDA pin needs to be externally pulled up.

GW1N-1P5

Table 12 GW1N-1P5 Configuration Modes

Package	JTAG	AUTO BOOT	I²C	SSPI	MSPI	DUAL BOOT	SERIAL	CPU
LQ100X[1]	Yes	Yes	Yes	No	No	No	No	No
LQ100	Yes	Yes	No	No	No	No	No	No
QN48X[1]	Yes	Yes	Yes	No	No	No	No	No

Note!

[1] When I2C is supported, the SDA and SCL pins need to be externally pulled up; when AUTOBOOT is supported, the SDA pin needs to be externally pulled up.

GW1N-4

Table 13 GW1N-4 Configuration Modes

Package	JTAG	AUTO BOOT	SSPI	MSPI	DUAL BOOT	SERIAL	CPU
QN32	Yes	Yes	No	Yes	No	No	No
QN48	Yes	Yes	No	Yes	No	No	No
CS72	Yes	Yes	Yes	No	No	No	No
QN88	Yes	Yes	No	Yes	No	No	No
LQ100	Yes	Yes	Yes	No	No	No	No
LQ144	Yes	Yes	Yes	Yes	No	No	No
MG132X	Yes	Yes	No	No	No	No	No
MG160	Yes	Yes	Yes	Yes	No	Yes	Yes
UG169	Yes	Yes	No	No	No	No	No
PG256	Yes	Yes	Yes	Yes	No	Yes	Yes
PG256M	Yes	Yes	Yes	Yes	No	Yes	Yes

GW1N-9

Table 14 GW1N-9 Configuration Modes

Package	JTAG	AUTO BOOT	SSPI	MSPI	DUAL BOOT	SERIAL	CPU
QN48	Yes	Yes	No	Yes	No	No	No
QN48F	Yes	Yes	Yes	No	No	No	No
QN88	Yes	Yes	No	Yes	No	No	No
CM64	Yes	Yes	No	No	No	No	No
CS81M	Yes	Yes	No	No	No	No	No
LQ100	Yes	Yes	Yes	No	No	No	No
LQ144	Yes	Yes	Yes	Yes	No	No	No
EQ144	Yes	Yes	Yes	Yes	No	No	No
MG160	Yes	Yes	Yes	Yes	Yes	Yes	Yes
LQ176	Yes	Yes	Yes	Yes	Yes	Yes	Yes
EQ176	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PG256	Yes	Yes	Yes	Yes	Yes	Yes	Yes
UG169	Yes	Yes	No	No	No	No	No
UG256	Yes	Yes	No	No	No	No	No
UG332	Yes	Yes	Yes	Yes	Yes	Yes	Yes
MG100	Yes	Yes	No	Yes	No	No	No
MG100T	Yes	Yes	No	No	No	No	No
MG196	Yes	Yes	No	No	No	No	No
QN60	Yes	Yes	No	Yes	No	No	No

GW1NR-1

Table 15 GW1NR-1 Configuaration Modes

Package	JTAG	AUTO BOOT	SSPI	MSPI	DUAL BOOT	SERIAL	CPU
FN32G	Yes	Yes	No	No	No	No	No
QN32X	Yes	Yes	No	No	No	No	No
QN48X	Yes	Yes	No	No	No	No	No
EQ144G	Yes	Yes	Yes	No	No	No	No
LQ100G	Yes	Yes	No	No	No	No	No

GW1NR-2

Table 16 GW1NR-2 Configuration Modes

Package	JTAG	AUTO BOOT	I^2C	SSPI	MSPI	DUAL BOOT	SERIAL	CPU
MG49P	Yes	Yes	Yes	No	No	No	No	No
MG49PG	Yes	Yes	Yes	No	No	No	No	No
MG49G	Yes	Yes	Yes	No	No	No	No	No

GW1NR-4

Table 17 GW1NR-4 Configuration Modes

Package	JTAG	AUTO BOOT	SSPI	MSPI	DUAL BOOT	SERIAL	CPU
QN88	Yes	Yes	No	Yes	No	No	No
MG81	Yes	Yes	No	Yes	No	No	No

GW1NR-9

Table 18 GW1NR-9 Configuration Modes

Package	JTAG	AUTO BOOT	SSPI	MSPI	DUAL BOOT	SERIAL	CPU
QN88	Yes	Yes	No	Yes	No	No	No
QN88P	Yes	Yes	No	Yes	No	No	No
LQ144P	Yes	Yes	Yes	Yes	No	No	No
MG100P	Yes	Yes	No	No	No	No	No
MG100PF	Yes	Yes	No	No	No	No	No
MG100PA	Yes	Yes	No	No	No	No	No
MG100PT	Yes	Yes	No	No	No	No	No
MG100PS	Yes	Yes	No	No	No	No	No

Pinout

Before designing circuits, users should take the overall FPGA pinout needs into consideration and make informed decisions related to the application of the device architecture features, including I/O LOGIC, global clock resources, PLL resources, etc.

For the distribution of True LVDS, refer to GW1N/GW1NR FPGA Product Pinout.

To support SSTL, HSTL, etc., each bank also provides one independent voltage source (V_{REF}) as the reference voltage. Users can choose V_{REF} from the internal reference voltage of the bank (0.5 x VCCIO) or external reference voltage V_{REF} using any I/O from the bank.

Note!

During configuration, all GPIOs of the device are high-impedance with internal weak pull-ups. After the configuration is complete, the I/O state is controlled by user programs and constraints. The state of CONFIG-related I/Os varies depending on the configuration mode.

Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

Revision History

Date	Version	Description
12/13/2016	1.0E	Initial version.
01/02/2018	1.1E	Related content added as follows: ● Dual-purpose pin ● FPGA external crystal oscillator circuit reference ● GW1NR bank voltage ● Configuration modes supported by each device.
04/23/2018	1.2E	Modify the power-on time reference range as "0.2ms~2ms" and add the remark information.
06/29/2018	1.3E	Revise the schematic diagram style uniformly.
04/03/2019	1.4E	The description of FASTRD_N updated.
04/12/2019	1.5E	The description added: The device I/Os (except TCK) are all internal weak pull-up.
05/10/2019	1.6E	Pull-down resistance for MCLK signal added.
06/04/2019	1.7E	Bank Voltage description updated.
01/24/2022	1.8E	● The value described in Recommended Operating Range fixed. ● The configuration modes supported by each device updated.
03/07/2022	1.8.1E	The configuration modes supported by each device updated.
03/25/2022	1.8.2E	The configuration modes supported by each device updated.
07/15/2022	1.8.3E	The note in "JTAG Download" updated.
07/22/2022	1.8.4E	The configuration modes supported by each device updated.
08/19/2022	1.8.5E	The note in "Pinout" updated.
09/20/2022	1.9E	"Power Supply" updated.
10/18/2022	1.9.1E	Recommended Reference Range of Power-up Time in "Power Supply" updated.
11/17/2022	1.9.2E	Recommended Reference Range of Power-up Time in "Power Supply" updated.
02/02/2023	1.9.3E	“Figure 3 JTAG Circuit Reference” in “JTAG Download” updated.
03/10/2023	1.9.4E	● The note of LVDS in “Differential Pin” updated. ● “Pinout” updated. ● The data of GW1N-4 example in “Power Supply Ramping Rate” updated.
06/30/3023	1.9.5E	● QN60 package added to the “Table 14 GW1N-9 Configuration

Date	Version	Description
		Modes” in “Configuration Modes Supported by Each Device”. ● The overview in “MODE” updated.
08/10/2023	1.9.6E	The note in “Pinout” optimized.
08/18/2023	1.9.7E	The “Table 14 GW1N-9 Configuration Modes” in “Configuration Modes Supported by Each Device” updated, QN60 supports MSPI mode.

Disclaimer

GOWINSEMI assumes no liability and provides no warranty (either expressed or implied) and is not responsible for any damage incurred to your hardware, software, data, or property resulting from usage of the materials or intellectual property except as outlined in the GOWINSEMI Terms and Conditions of Sale. GOWINSEMI may make changes to this document at any time without prior notice. Anyone relying on this documentation should contact GOWINSEMI for the current documentation and errata.