DK-START-GW2A18

User Guide

DBUG354-1.0E,08/28/2018

Disclaimer

Revision History

Date	Version	Description
08/28/2018	1.0E	Initial version published.

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1 About This Guide

1.1 Purpose

The DK-START-GW2A18 development board (hereinafter referred to as development board) user manual consists of the following four parts:

1. A brief introduction to the features and hardware resources of the development board;
2. An introduction to the development board architecture and hardware resources;
3. An introduction to the hardware circuit functions, circuits, and pins distribution;
4. An introduction to the use of the Gowin YunYuan software.

1.2 Supported Products

The information presented in this guide applies to the following Gowin FPGA products:

GW2A-LV18PG256.

1.3 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

1. GW2A series of FPGA Products Data Sheet
2. GW2A-18 Pinout
3. GW2A series of FPGA Products Package and Pinout

1.4 Abbreviations and Terminology

The abbreviations and terminology used in this manual are set out in Table 1-1 below.

Table 1-1 Abbreviations and Terminology

Abbreviations and Terminology	Full Name
B-SRAM	Block SRAM
DDR	Double-Data-Rate Synchronous Dynamic Random Access Memory
DSP	Digital Signal Processing
FLASH	Flash Memory
FPGA	Field Programmable Gate Array
GPIO	General Purpose Input Output
LDO	Low Dropout Regulator
LUT4	4-input Look-up Tables
LVDS	Low-Voltage Differential Signaling
S-SRAM	Shadow SRAM

1.5 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

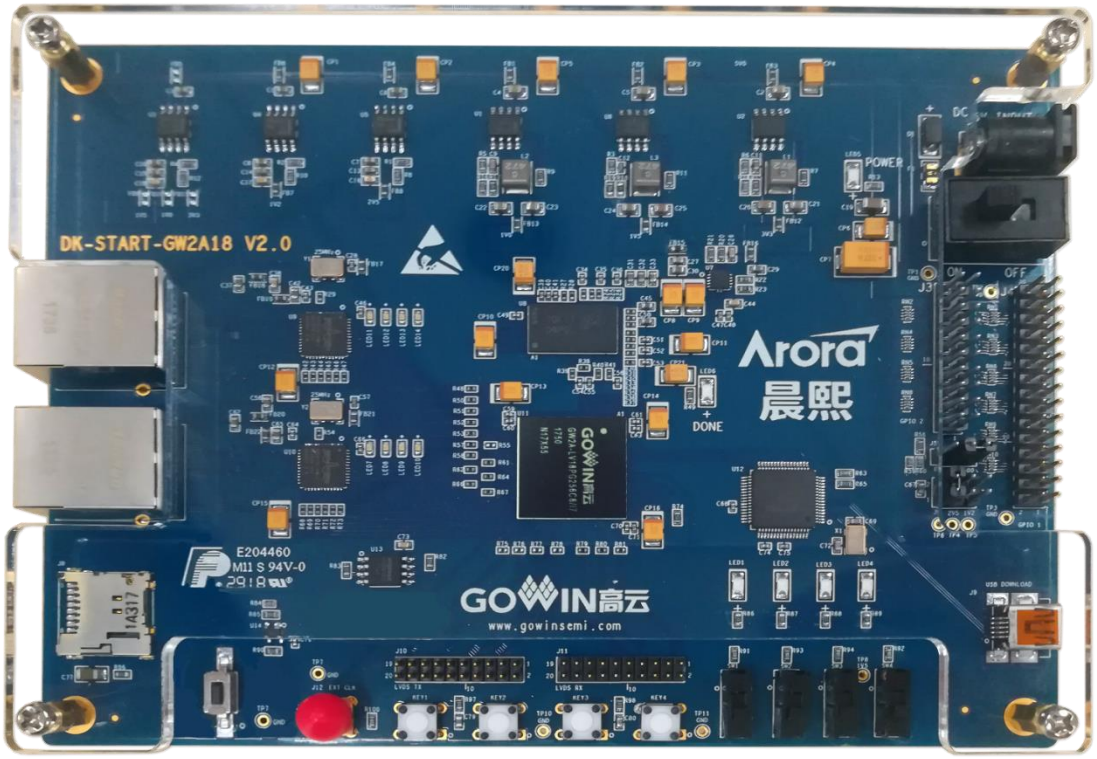
E-mail: support@gowinsemi.com

+Tel: 86 -20 -8757 -8868

2 Development Board Description

2.1 Overview

Figure 2-1 DK-START-GW2A18



DK-START-GW2A18 applies to high speed data storage, high-speed communication test, FPGA functions evaluation, the verification of hardware reliability, software learning and debugging, etc.

The development board uses the GW2A-LV18PG256 FPGA device, which is the first generation products of Gowin Arora ® family. The GW2A series of FPGA products offer a range of comprehensive features and rich internal resources like high-performance DSP resources, a high-speed

LVDS interface, and abundant BSRAM memory resources. These embedded resources combine a streamlined FPGA architecture with a 55nm process to make the GW2A series of FPGA products ideal for high-speed and low-cost applications.

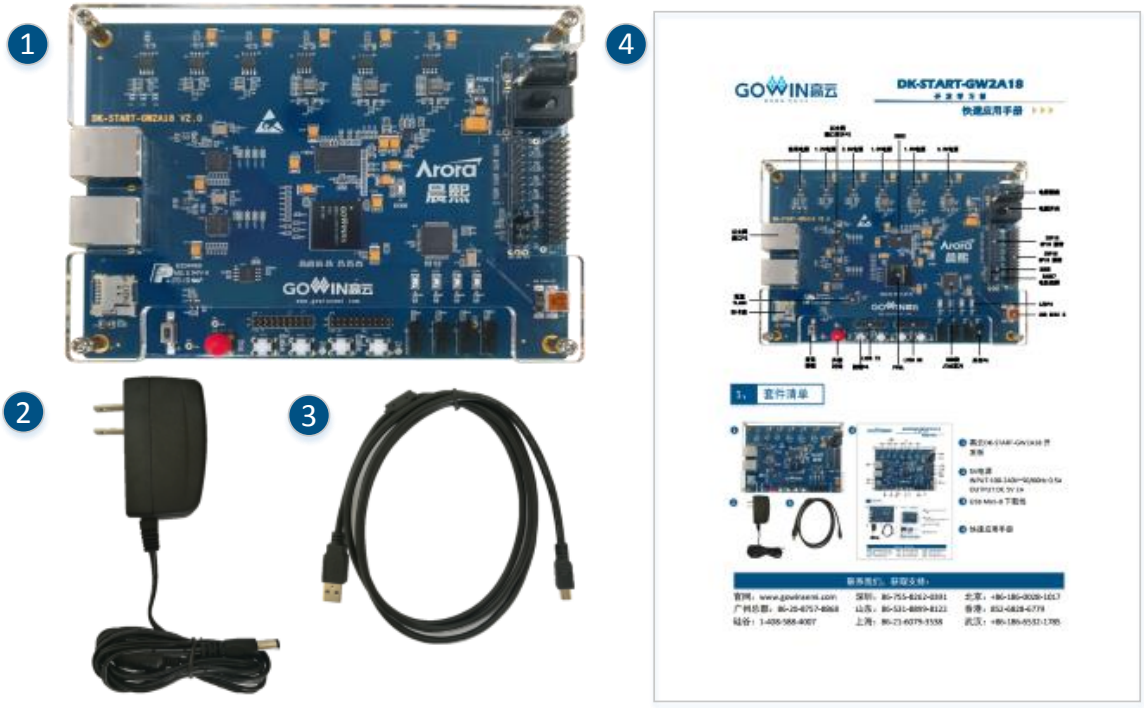
DK-START-GW2A18 includes a DDR3 chip with 2Gbit storage space,16 bits data bus width, and the highest data speed of 1600MT/s. Its two Gigabit Ethernet interfaces support 10M,100M,1000M Ethernet communication. It has abundant peripheral interfaces, including LVDS interfaces, a SD card slot, and GPIO interfaces. Besides that, it also offers an external Flash, slide switches, key switches, external clocks, etc.

2.2 A Development Board Suite

A development board suite includes the following items:

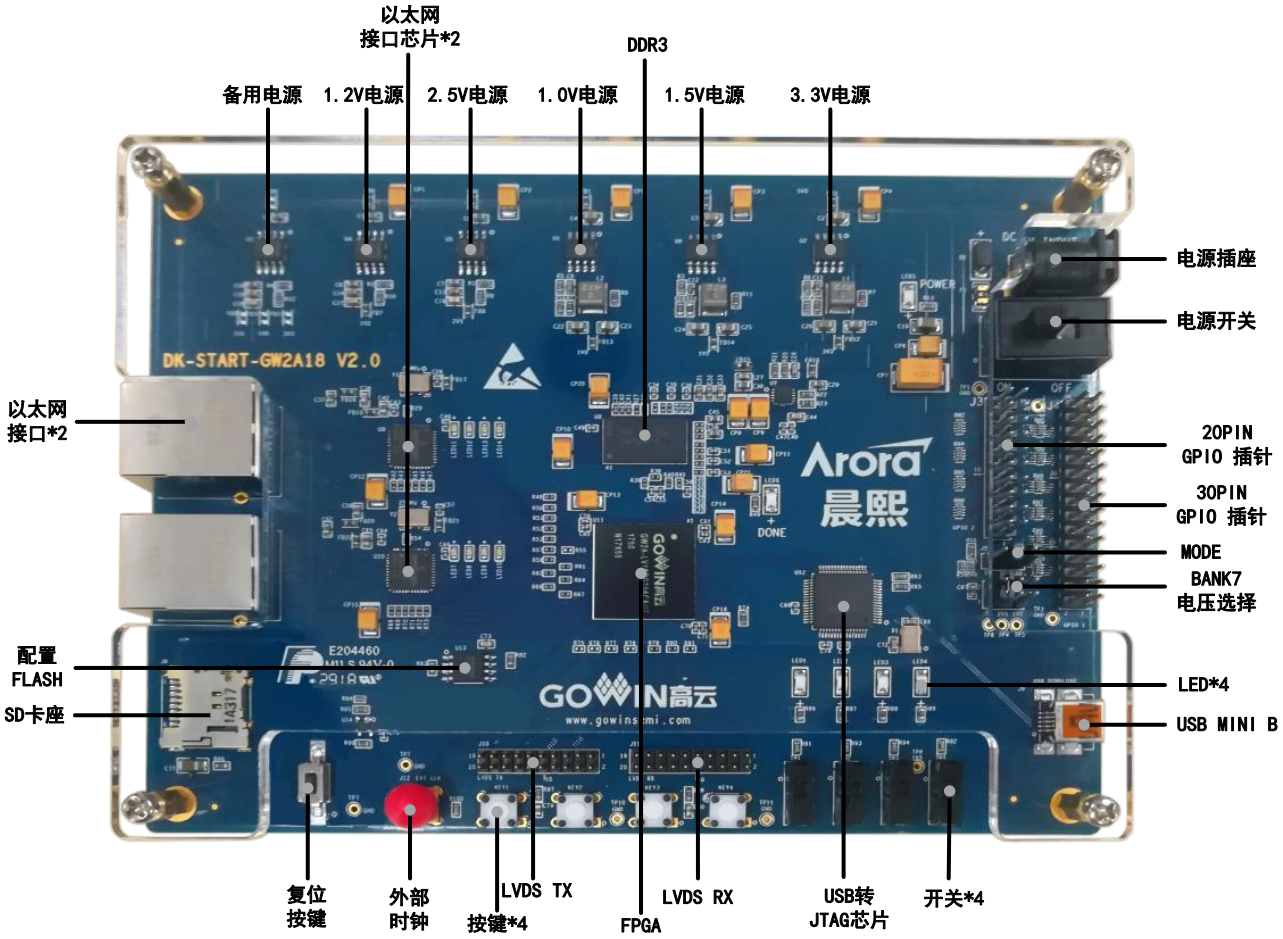
1. DK-START-GW2A
2. 5V power (Input: 100-240V~50/60Hz 0.5A, output: DC 5V 2A)
3. USB Mini B cable
4. Quick Start

Figure 2-2 A Development Board Suite



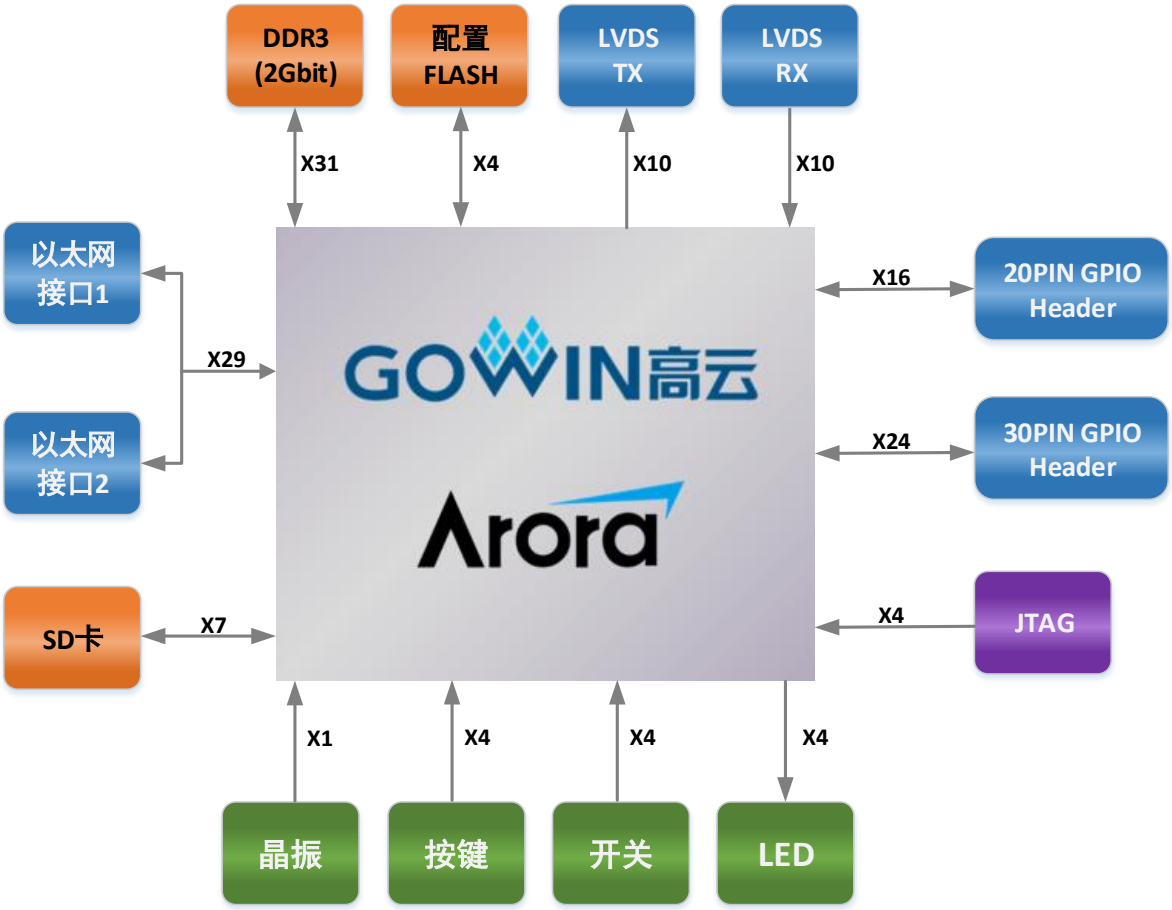
2.3 PCB Components

Figure 2-1 PCB Components



2.4 System Architecture

Figure 2-2System Architecture



2.5 Features

The key features of DK-START-GW2A is as follows:

1. The FPGA device
   - GW2A-LV18PG256C8/I7
   - Max. user I/O 207
2. Download and Boot
   - Integrates the download module; can be downloaded with the USB Mini B cable
   - External Flash boot
   - The blue DONE light is on after loading
3. Power
   - External 5V 2A Power supply

- The blue POWER light is on after power on
- The development board generates 3.3V, 2.5V, 1.5V, 1.2V, 1.0V, and 0.75V (required by DDR3)

4. Clock system
   - 50MHz crystal oscillator Input
   - External signals input
5. Memory device
   - 2Gbit DDR3 SDRAM
   - 64Mbit FLASH
6. Ethernet interface
   - Two Ethernet interfaces
   - Supports 10M/100M/1000M
   - RJ45 connector with built-in transformer
7. LVDS interfaces;
   - One LVDS interface for receiving, including five pairs of differential signals.
   - One LVDS interface for sending, including five pairs of differential signals.
   - The receiving/sending functions can be modified by changing the resistance.

   Note！

   For the V2.0 development board, J13 needs to be set as 2.5V when LVDS is used.
8. SD card slot
   - Eight contacts, push-push type
   - Card detection
9. Extension interface
   - 20PIN double row pins, including 16 GPIO, one I/O Bank voltage (can be adjusted as 3.3V, 2.5V, 1.2V), one 3.3V voltage, one 5V voltage, and two ground pins.
   - 30PIN double row pins, including 24 GPIO, one 2.5V I/O Bank voltage, one 3.3V voltage, one 5V voltage, and three ground pins.

   Note!

   For the V2.0 development board, the BANK0 voltage and BANK1 voltage can be set as 3.3V or 2.5V using J13.
10. Debugging module
    - Four keys
    - Four switches

- Four blue LEDs

3 Development Board Circuit

3.1 FPGA Module

3.1.1 Introduction

The resources of GW2A-LV18PG256 FPGA are set out in Table 3-1.

Table 3-1GW2A-LV18PG256 FPGA Resources List

Device	GW2A-LV18PG256
LUT4	20,736
Flip-Flop (FF)	15,552
Shadow SRAM S-SRAM (bits)	41,472
Block SRAM B-SRAM(bits)	828K
B-SRAM quantity B-SRAM	46
18 x 18 Multiplier	48
PLLs+DLLs	4+4
Total number of I/O banks	8
Max. User I/O	207
Core voltage	1.0V

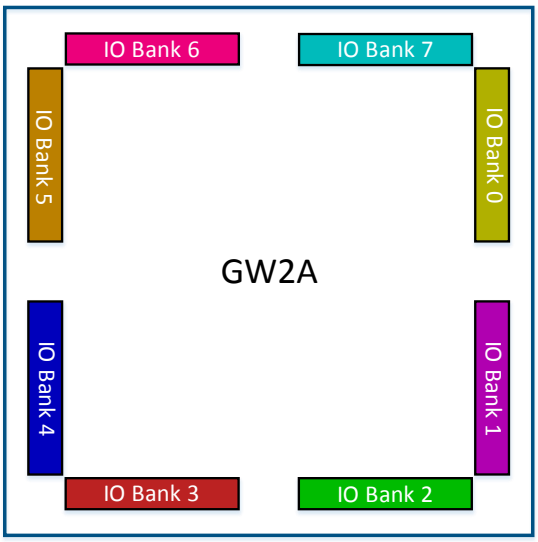
Note!

See *GW2A series of FPGA Products Data Sheet* for further details.

3.1.2 I/O Distribution

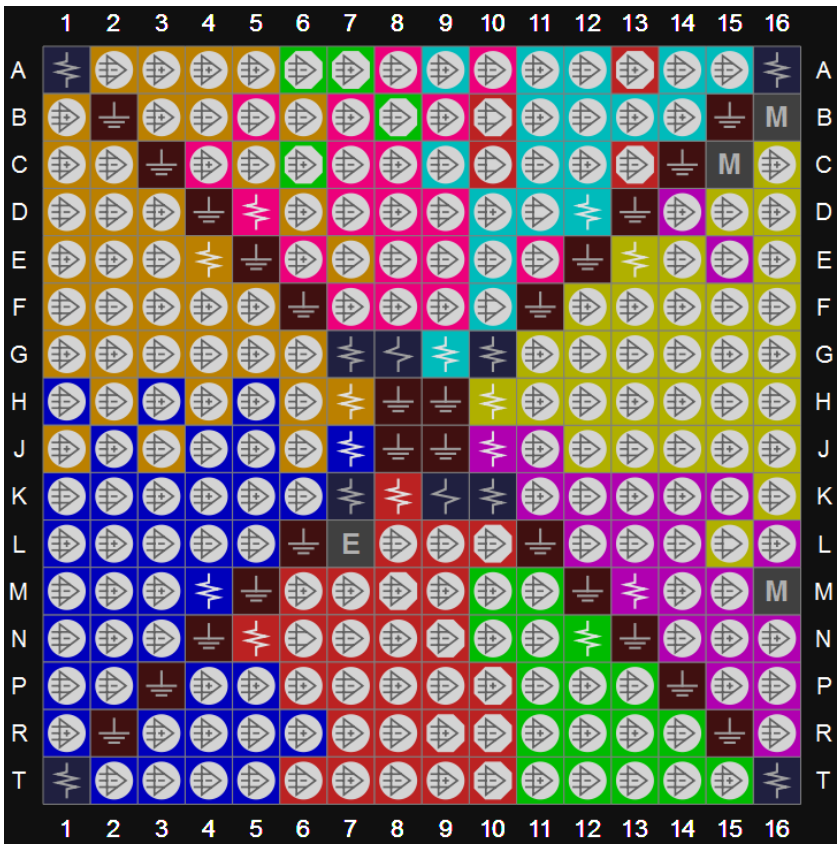
GW2A series FPGA products includes eight I/O Bank. The I/O Bank Distribution is as shown in Figure 3-1.

Figure 3-1 GW2A I/O Bank Distribution



The view of GW2A-18 PG256 pins distribution is as shown in Figure 3-2.

Figure 3-2 View of GW2A-18 PG256 Pins Distribution (Top View)



The board I/O Bank and functions are as listed in Table 3-2.

Table 3-2 FPGA I/O Bank Voltage and Functions

I/O BANK No.	Supply voltage	Functions
BANK0	2.5V[1]	LVDS_RX Interface 30PIN GPIO Interface 50MHz crystal oscillator Input LED
BANK1	2.5V[1]	LVDS_TX Interface 30PIN GPIO Interface
BANK2	3.3V	Ethernet interface1 Ethernet interface2 JTAG Download SD card slot External Clock
BANK3	3.3V	Ethernet interface2 FLASH Configuration SD card slot Reset MODE

I/O BANK No.	Supply voltage	Functions
		DONE RECONFIG_N READY FASTRD_N
BANK4	1.5V	DDR3 Key
BANK5	1.5V	DDR3
BANK6	1.5V	DDR3 Switches
BANK7	3.3V, 2.5V, 1.2V (Adjustable)	20PIN GPIO Interface

Note！

For the V2.0 development board, the BANK0 voltage and BANK1 voltage can be set as 3.3V or 2.5V using J13.

3.2 Download Module

3.2.1 Introduction

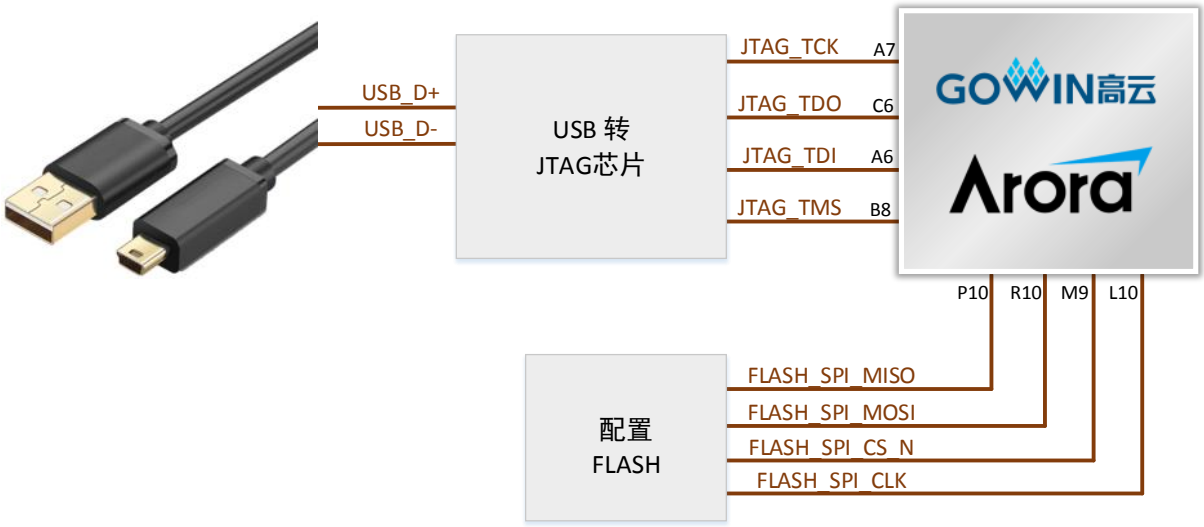
The development board offers a USB download interface. You can set the MODE value to download the programs to the on-chip SRAM or external Flash. When downloaded to SRAM, the data stream file will be lost if the device is power down. When downloaded to Flash, the data stream file will not be lost.

The MODE value configuration:

1. In any modes, you can download the data stream file to the on-chip SRAM and run it immediately.
2. Set MODE as "000" to download the data stream file to the external Flash. When power-on again, the device will read the FPGA configuration data from the Flash automatically.

The connection diagram for downloading and configuration is as follows:

Figure 3-3 Connection Diagram for FPGA Downloading and Configuration



3.2.2 Pins Distribution

Table 3-3 FPGA Download and Pins Distribution

Signal Name	FPGA Pin No.	BANK	I/O	Description
JTAG_TCK	A7	2	3.3V	JTAG Signal
JTAG_TDO	C6	2	3.3V	JTAG Signal
JTAG_TDI	A6	2	3.3V	JTAG Signal
JTAG_TMS	B8	2	3.3V	JTAG Signal
FLASH_SPI_MISO	P10	3	3.3V	FLASH signals configuration
FLASH_SPI_MOSI	R10	3	3.3V	FLASH signals configuration
FLASH_SPI_CS_N	M9	3	3.3V	FLASH signals configuration
FLASH_SPI_CLK	L10	3	3.3V	FLASH signals configuration

3.3 Power Supply

3.3.1 Introduction

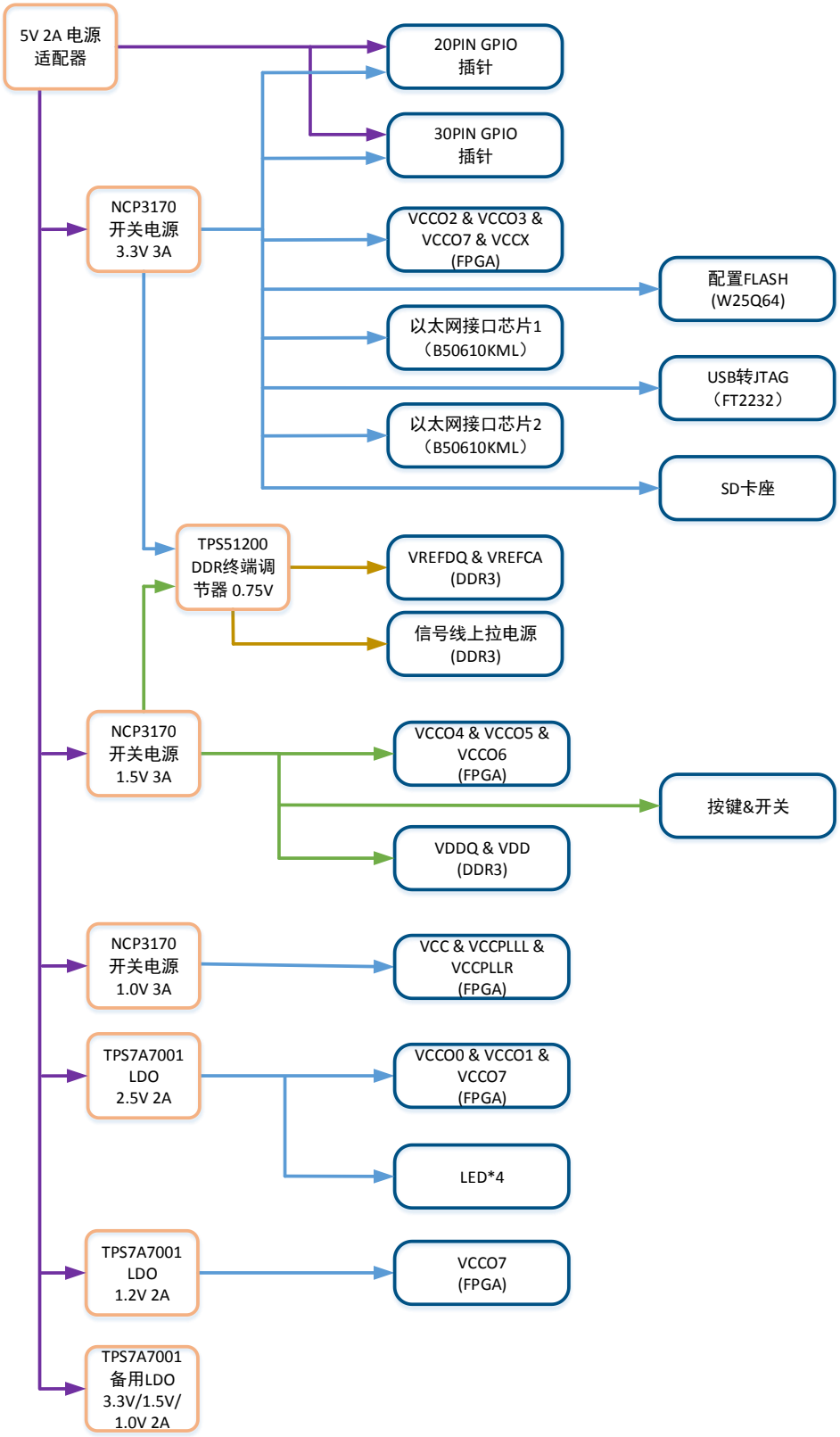
5V power (Input: 100-240V~50/60MHz 0.5A, output: DC +5V 2A) The development board generates 3.3V, 2.5V, 1.5V, 1.2V, 1.0V, and 0.75V (required by DDR3).

One redundant power location is reserved on the development board. A LDO can be welded to generate 3.3V, 1.5V, and 1.0V. The rated current

is 2A. When the redundant power is used to replace the main power, you need to take off the main power's magnetic beads to avoid the power conflicts.

3.3.2 Power System Distribution

Figure 3-4 Power System Distribution



Note ! For the V2.0 development board, the BANK0 voltage and BANK1 voltage can be set as 3.3V or 2.5V using J13.

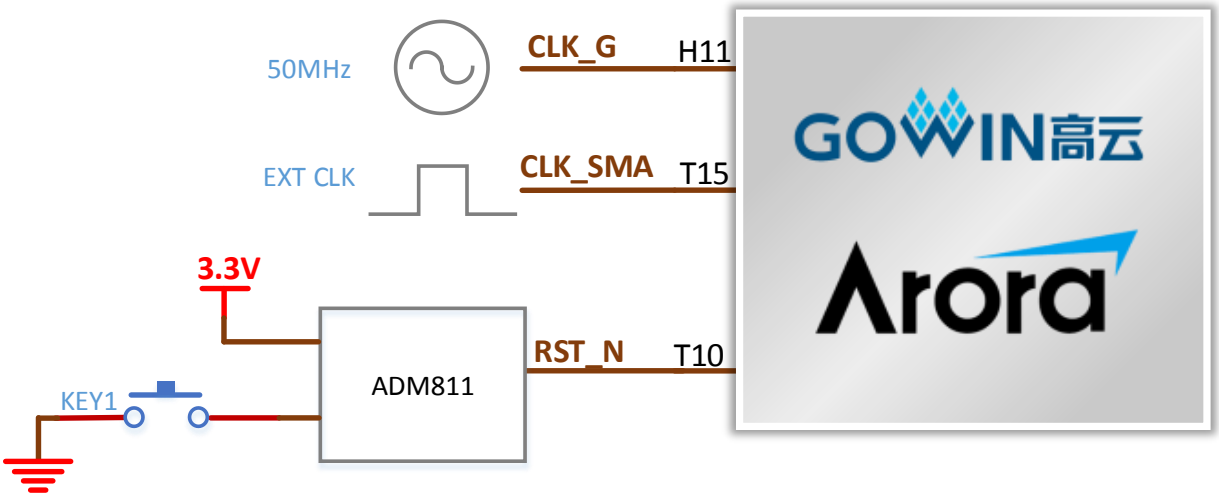
3.4 Clock, Reset

3.4.1 Introduction

The development board offers a 50MHz oscillator, connecting to the global clock pins. It also offers a female SMA seat for users to input the external clock for multiple tests.

The reset circuit adopts keys and dedicated reset chips. After powered on the device, the reset chip automatically generates a reset signal to reset the FPGA and Ethernet PHY chip. The 3.3V voltage is monitored in real time. The reset signal will be generated once an exception occurs. The reset signal can also be generated via the reset key.

Figure 3-5 Connection Diagram for Clock and Reset



3.4.2 Pins Distribution

Table 3-4 Clock and Reset Pins Distribution

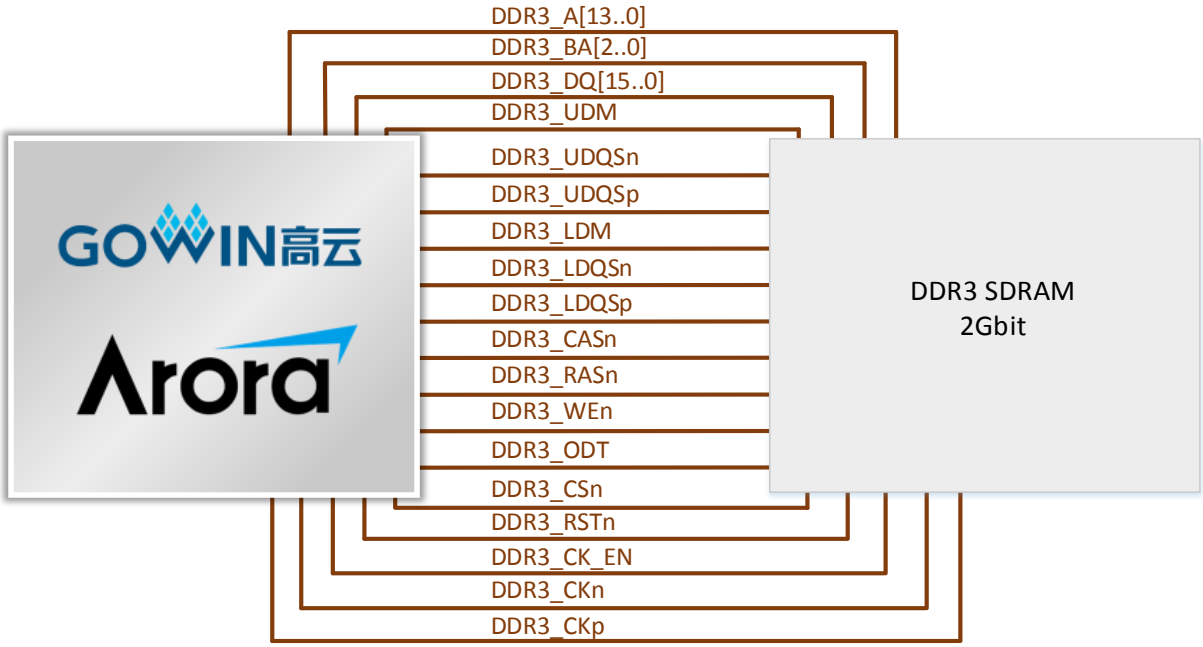
Signal Name	FPGA Pin No.	BANK	I/O	Description
CLK_G	H11	0	2.5V	50MHz crystal oscillator Input
CLK_SMA	T15	2	3.3V	External clock input
RST_N	T10	3	3.3V	Reset signal, active low

3.5 DDR3

3.5.1 Introduction

The development board includes a DDR3 chip with 2Gbit storage space,16 bits data bus width, and the highest data speed of 1600MT/s.

Figure 3-6 Connection Diagram of FPGA and DDR3



3.5.2 Pins Distribution

Table 3-5 DDR3 Pins Distribution

Signal Name	FPGA Pin No.	BANK	I/O	Description
DDR3_A0	F7	6	1.5V	Address
DDR3_A1	A4	5	1.5V	Address
DDR3_A2	D6	5	1.5V	Address
DDR3_A3	F8	6	1.5V	Address
DDR3_A4	C4	6	1.5V	Address
DDR3_A5	E6	6	1.5V	Address
DDR3_A6	B1	5	1.5V	Address
DDR3_A7	D8	6	1.5V	Address
DDR3_A8	A5	5	1.5V	Address
DDR3_A9	F9	6	1.5V	Address
DDR3_A10	K3	4	1.5V	Address
DDR3_A11	B7	6	1.5V	Address
DDR3_A12	A3	5	1.5V	Address

Signal Name	FPGA Pin No.	BANK	I/O	Description
DDR3_A13	C8	6	1.5V	Address
DDR3_BA0	H4	5	1.5V	Bank address
DDR3_BA1	D3	5	1.5V	Bank address
DDR3_BA2	H5	4	1.5V	Bank address
DDR3_CASn	R6	4	1.5V	Column address strobe
DDR3_CK_EN	J2	4	1.5V	Clock Enable
DDR3_CKn	J3	5	1.5V	Differential clock
DDR3_CKp	J1	5	1.5V	Differential clock
DDR3_CSn	P5	4	1.5V	Chip select
DDR3_DQ0	G5	5	1.5V	Data
DDR3_DQ1	F5	5	1.5V	Data
DDR3_DQ2	F4	5	1.5V	Data
DDR3_DQ3	F3	5	1.5V	Data
DDR3_DQ4	E2	5	1.5V	Data
DDR3_DQ5	C1	5	1.5V	Data
DDR3_DQ6	E1	5	1.5V	Data
DDR3_DQ7	B3	5	1.5V	Data
DDR3_DQ8	M3	4	1.5V	Data
DDR3_DQ9	K4	4	1.5V	Data
DDR3_DQ10	N2	4	1.5V	Data
DDR3_DQ11	L1	4	1.5V	Data
DDR3_DQ12	P4	4	1.5V	Data
DDR3_DQ13	H3	4	1.5V	Data
DDR3_DQ14	R1	4	1.5V	Data
DDR3_DQ15	M2	4	1.5V	Data
DDR3_LDM	G1	5	1.5V	Data input mask
DDR3_LDQSn	G3	5	1.5V	Data strobe
DDR3_LDQSp	G2	5	1.5V	Data strobe
DDR3_ODT	R3	4	1.5V	On-Die Termination Enable
DDR3_RASn	R4	4	1.5V	Row address strobe
DDR3_RSTn	B9	6	1.5V	Reset
DDR3_UDM	K5	4	1.5V	Data input mask

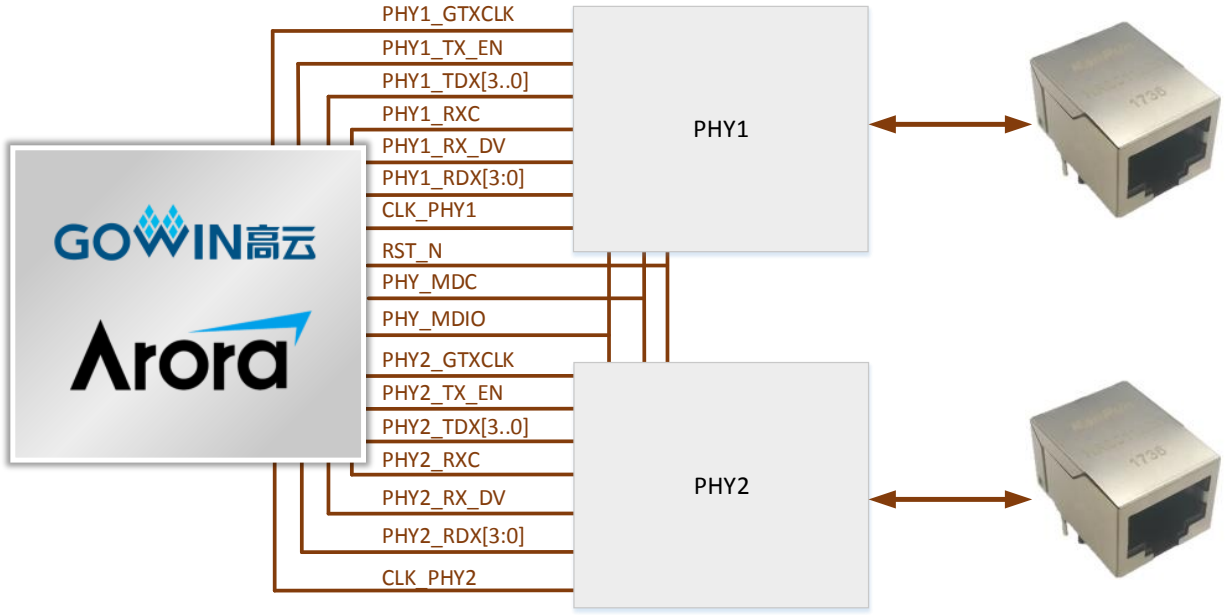
Signal Name	FPGA Pin No.	BANK	I/O	Description
DDR3_UDQSn	K6	4	1.5V	Data strobe
DDR3_UDQSp	J5	4	1.5V	Data strobe
DDR3_WEn	L2	4	1.5V	Write enable

3.6 Ethernet interface

3.6.1 Introduction

The development board has two Ethernet circuits and supports gigabit mode, which can be used to test hardware environment in the LED display applications, and Ethernet data transmission. The interface connected to other devices is RJ45 with the built-in transformer. The connection diagram is as follows:

Figure 3-7 Connection Diagram of FPGA and Ethernet



3.6.2 Pins Distribution

Table 3-6 Ethernet Pins Distribution

Signal Name	FPGA Pin No.	BANK	I/O	Description
PHY_MDC	M10	2	3.3V	Management channel clock
PHY_MDIO	N11	2	3.3V	Manage channel data
PHY1_GTXCLK	N10	2	3.3V	PHY1 Transmitter Clock
PHY1_TXD0	P11	2	3.3V	PHY1 sending data channel 0
PHY1_TXD1	P12	2	3.3V	PHY1 sending data channel1

Signal Name	FPGA Pin No.	BANK	I/O	Description
PHY1_TXD2	P13	2	3.3V	PHY1 sending data channel 2
PHY1_TXD3	T11	2	3.3V	PHY1 sending data channel 3
PHY1_TX_EN	R11	2	3.3V	PHY1 sending data enable
PHY1_RXC	T12	2	3.3V	PHY1 Clock receive
PHY1_RXD0	R12	2	3.3V	PHY1 receive data channel 0
PHY1_RXD1	T13	2	3.3V	PHY1 receive data channel 1
PHY1_RXD2	R13	2	3.3V	PHY1 receive data channel 2
PHY1_RXD3	T14	2	3.3V	PHY1 receive data channel 3
PHY1_RX_DV	R14	2	3.3V	PHY1 receive data enable
PHY2_GTCLK	T7	3	3.3V	PHY2 Transmitter Clock
PHY2_TXD0	M6	3	3.3V	PHY2 sending data channel 0
PHY2_TXD1	N6	3	3.3V	PHY2 sending data channel 1
PHY2_TXD2	P6	3	3.3V	PHY2 sending data channel 2
PHY2_TXD3	M7	3	3.3V	PHY2 sending data channel 3
PHY2_TX_EN	P8	3	3.3V	PHY2 sending data enable
PHY2_RXC	N7	3	3.3V	PHY2 Clock receive
PHY2_RXD0	P7	3	3.3V	PHY2 receive data channel 0
PHY2_RXD1	R7	3	3.3V	PHY2 receive data channel 1
PHY2_RXD2	R8	3	3.3V	PHY2 receive data channel 2
PHY2_RXD3	T8	3	3.3V	PHY2 receive data channel 3
PHY2_RX_DV	T9	3	3.3V	PHY2 receive data enable

3.7 LVDS interfaces

3.7.1 Introduction

The LVDS interfaces are the two 20 contact pins with the pitch of 2.00mm. One defaults to the transmitting interface. The other one defaults to the receiving interface. Each interface includes five pairs of differential signals. The terminating resistor can be changed to modify the transmitting and receiving attributes, as shown in the figure below.

Figure 3-8 LVDS TX Interface

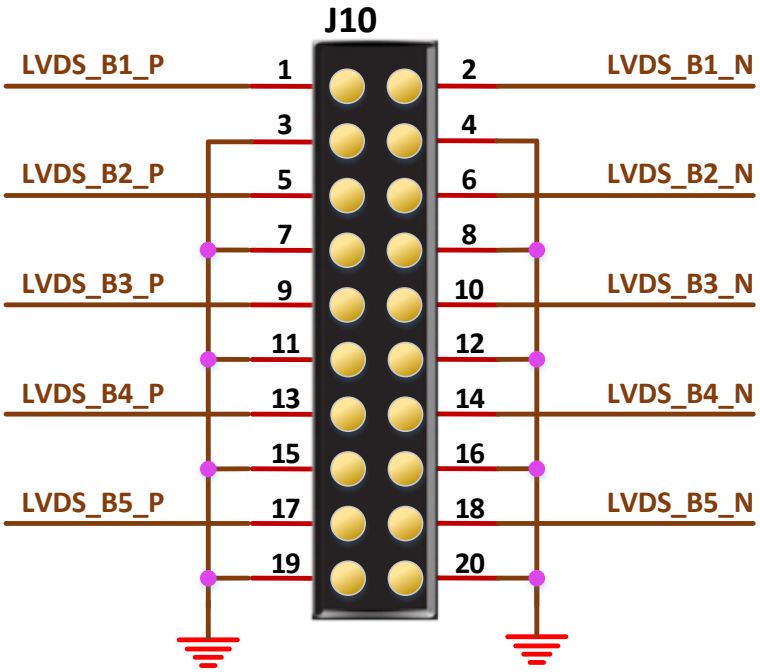
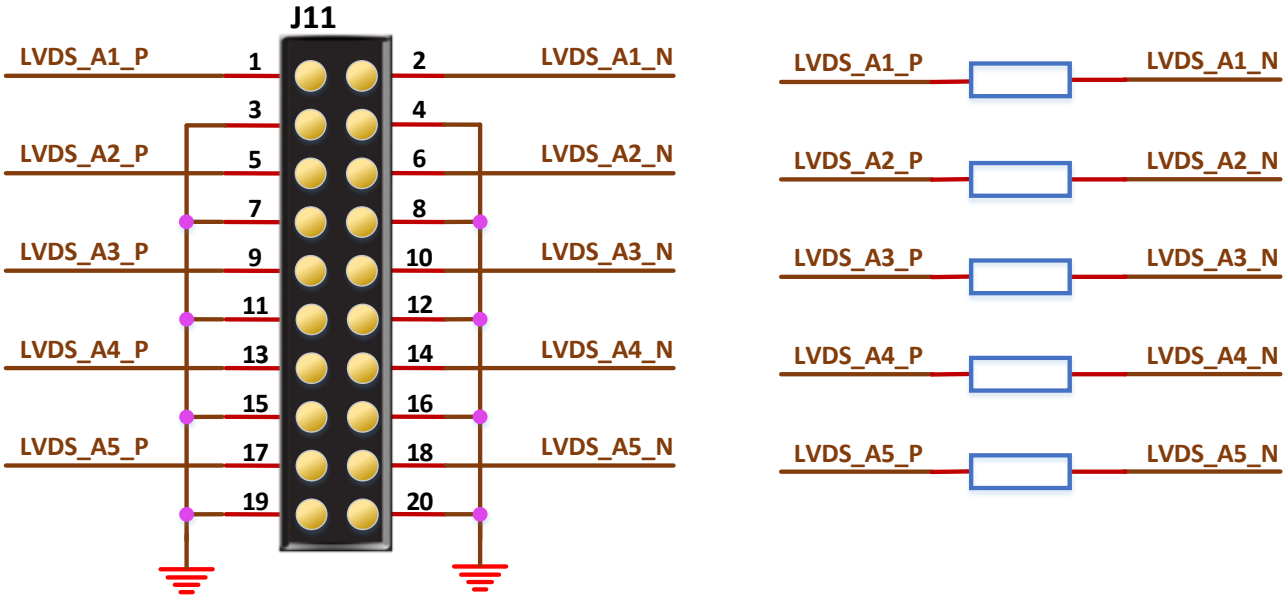


Figure 3-9 LVDS RX Interface



3.7.2 Pins Distribution

Table 3-7 LVDS TX Interface Pins Distribution

Pins Number	Signal Name	FPGA Pin No.	BANK	I/O	Description
1	LVDS_B1_P	K14	1	2.5V	Differential Channel 1+
2	LVDS_B1_N	K15	1	2.5V	Differential Channel 1-
5	LVDS_B2_P	L16	1	2.5V	Differential Channel 2+
6	LVDS_B2_N	L14	1	2.5V	Differential Channel 2-
9	LVDS_B3_P	N16	1	2.5V	Differential Channel 3+
10	LVDS_B3_N	N14	1	2.5V	Differential Channel 3-
13	LVDS_B4_P	N15	1	2.5V	Differential Channel 4+
14	LVDS_B4_N	P16	1	2.5V	Differential Channel 4-
17	LVDS_B5_P	P15	1	2.5V	Differential Channel 5+
18	LVDS_B5_N	R16	1	2.5V	Differential Channel 5-

For the V2.0 development board, J13 needs to be set as 2.5V when LVDS is used.

Table 3-8 LVDS RX Interface Pins Distribution

Pins Number	Signal Name	FPGA Pin No.	BANK	I/O	Description
1	LVDS_A1_P	D16	0	2.5V	Differential Channel 1+
2	LVDS_A1_N	E14	0	2.5V	Differential Channel 1-
5	LVDS_A2_P	E16	0	2.5V	Differential Channel 2+
6	LVDS_A2_N	F15	0	2.5V	Differential Channel 2-
9	LVDS_A3_P	G16	0	2.5V	Differential Channel 3+
10	LVDS_A3_N	H15	0	2.5V	Differential Channel 3-
13	LVDS_A4_P	H14	0	2.5V	Differential Channel 4+
14	LVDS_A4_N	H16	0	2.5V	Differential Channel 4-
17	LVDS_A5_P	J15	0	2.5V	Differential Channel 5+
18	LVDS_A5_N	K16	0	2.5V	Differential Channel 5-

For the V2.0 development board, J13 needs to be set as 2.5V when LVDS is used.

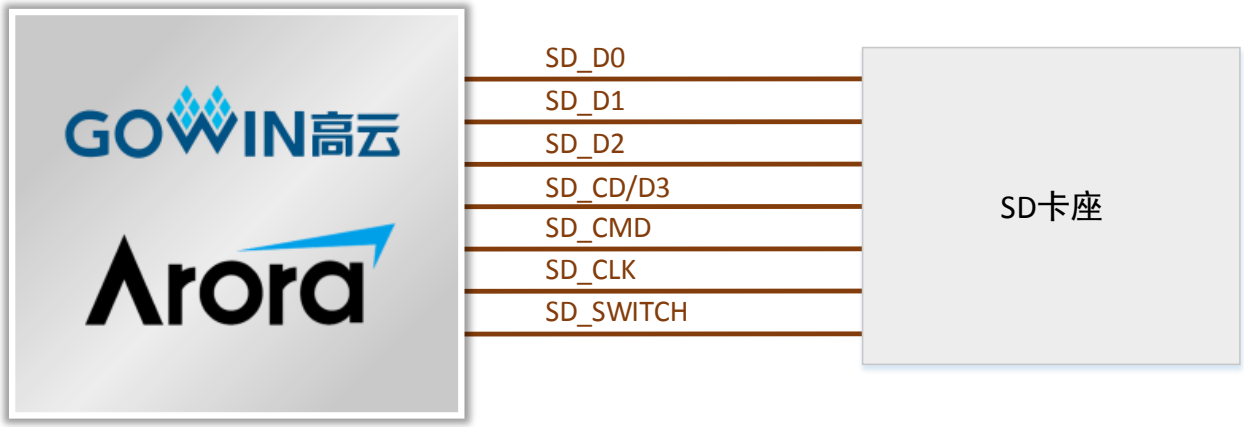
3.8 SD Card

3.8.1 Introduction

The SD card slot on the board is the push-push type with eight

contacts. It offers the detection of the card insertion. The connection diagram is shown as follows.

Figure 3-10 Connection Diagram of SD Card



3.8.2 Pins Distribution

Table 4-3 SD Card Pins Distribution

Signal Name	FPGA Pin No.	BANK	I/O	Description
SD_D0	M8	3	3.3V	Data bits 0
SD_D1	N8	3	3.3V	Data bits 1
SD_D2	L9	3	3.3V	Data bits 2
SD_CD/D3	N9	3	3.3V	Card detection/Data bits 3
SD_CMD	P9	3	3.3V	Commands/Response
SD_CLK	L8	3	3.3V	Clock
SD_SWITCH	M11	2	3.3V	Insertion Detection

3.9 GPIO

3.9.1 Introduction

Two double row pins with the pitch of 2.54mm are reserved on the development board. The 20 pin interface connects to Bank7, and the I/O voltage can be adjusted as 3.3V, 2.5V, and 1.2V. The I/O voltage of the 30 pin can be set as 2.5V, as shown in the figure below.

Figure 3-11 20pin Interface

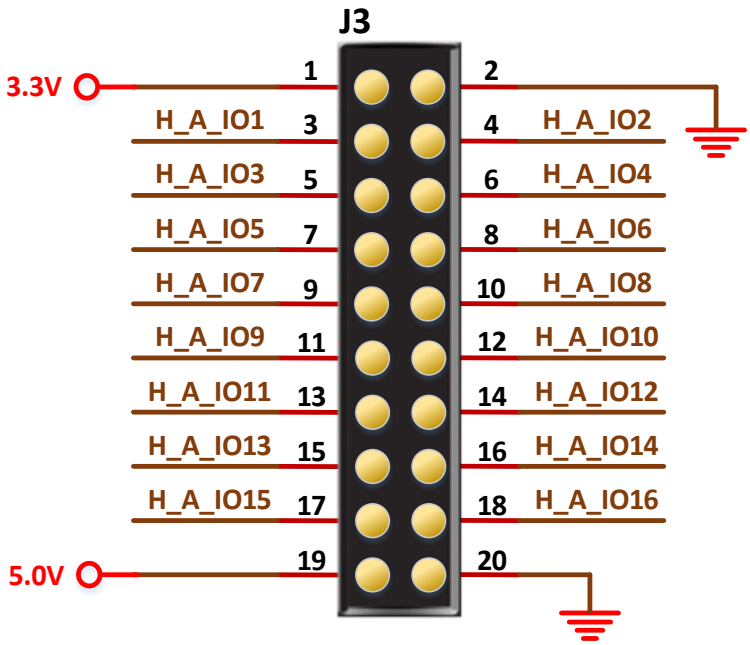
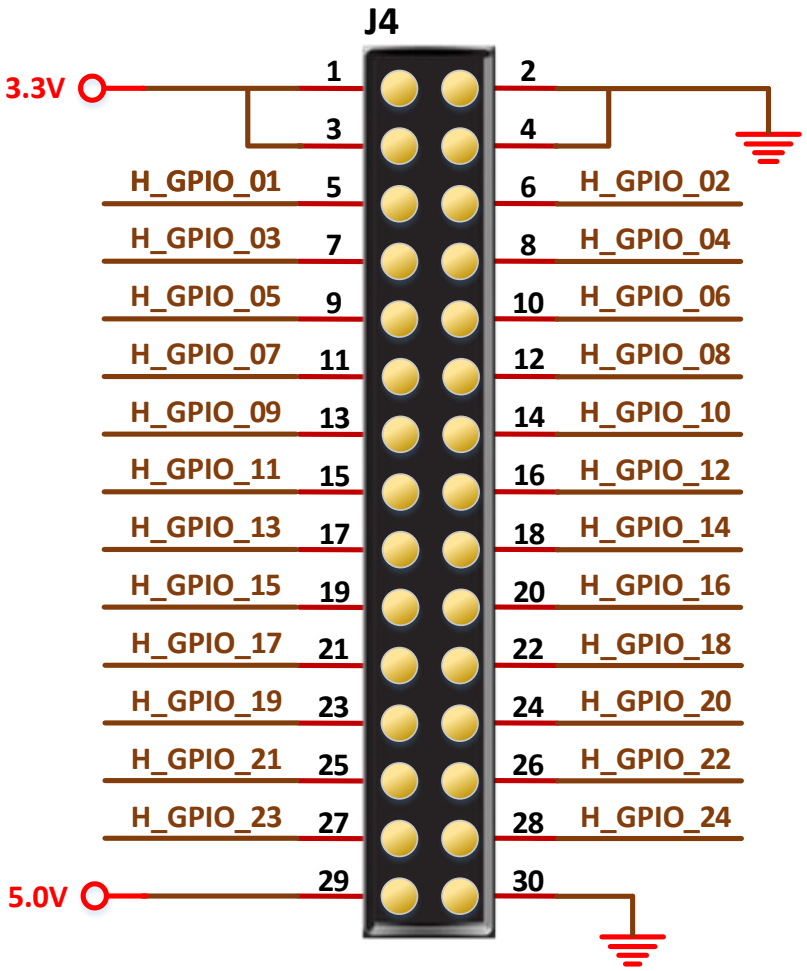


Figure 3-12 30pin Interface



3.9.2 Pins Distribution

Table 3-9 20pin Interface Pins Distribution

Pins Number	Signal Name	FPGA Pin No.	BANK	I/O	Description
3	H_A_IO1	A15	7	3.3V / 2.5V / 1.2V	General I/O
4	H_A_IO2	A14	7	3.3V / 2.5V / 1.2V	General I/O
5	H_A_IO3	B14	7	3.3V / 2.5V / 1.2V	General I/O
6	H_A_IO4	B13	7	3.3V / 2.5V / 1.2V	General I/O
7	H_A_IO5	C12	7	3.3V / 2.5V / 1.2V	General I/O
8	H_A_IO6	D11	7	3.3V / 2.5V / 1.2V	General I/O
9	H_A_IO7	A12	7	3.3V / 2.5V / 1.2V	General I/O
10	H_A_IO8	B12	7	3.3V / 2.5V / 1.2V	General I/O
11	H_A_IO9	C11	7	3.3V / 2.5V / 1.2V	General I/O
12	H_A_IO10	D10	7	3.3V / 2.5V / 1.2V	General I/O
13	H_A_IO11	A11	7	3.3V / 2.5V / 1.2V	General I/O
14	H_A_IO12	B11	7	3.3V / 2.5V / 1.2V	General I/O

Pins Number	Signal Name	FPGA Pin No.	BANK	I/O	Description
15	H_A_IO13	E10	7	3.3V / 2.5V / 1.2V	General I/O
16	H_A_IO14	C9	7	3.3V / 2.5V / 1.2V	General I/O
17	H_A_IO15	A9	7	3.3V / 2.5V / 1.2V	General I/O
18	H_A_IO16	F10	7	3.3V / 2.5V / 1.2V	General I/O

Table 3-10 30pin Interface Pins Distribution

Pins Number	Signal Name	FPGA Pin No.	BANK	I/O	Description
5	H_GPIO_01	M14	1	2.5V	General I/O
6	H_GPIO_02	K12	1	2.5V	General I/O
7	H_GPIO_03	J13	0	2.5V	General I/O
8	H_GPIO_04	H13	0	2.5V	General I/O
9	H_GPIO_05	G13	0	2.5V	General I/O
10	H_GPIO_06	L13	1	2.5V	General I/O
11	H_GPIO_07	L15	0	2.5V	General I/O
12	H_GPIO_08	M15	1	2.5V	General I/O
13	H_GPIO_09	J16	0	2.5V	General I/O
14	H_GPIO_10	L12	1	2.5V	General I/O
15	H_GPIO_11	K13	1	2.5V	General I/O
16	H_GPIO_12	K11	1	2.5V	General I/O
17	H_GPIO_13	J11	1	2.5V	General I/O
18	H_GPIO_14	J14	0	2.5V	General I/O
19	H_GPIO_15	J12	0	2.5V	General I/O
20	H_GPIO_16	G15	0	2.5V	General I/O
21	H_GPIO_17	E15	1	2.5V	General I/O
22	H_GPIO_18	C16	0	2.5V	General I/O
23	H_GPIO_19	D15	0	2.5V	General I/O
24	H_GPIO_20	D14	1	2.5V	General I/O
25	H_GPIO_21	G14	0	2.5V	General I/O
26	H_GPIO_22	H12	0	2.5V	General I/O
27	H_GPIO_23	F12	0	2.5V	General I/O
28	H_GPIO_24	G11	0	2.5V	General I/O

Note！

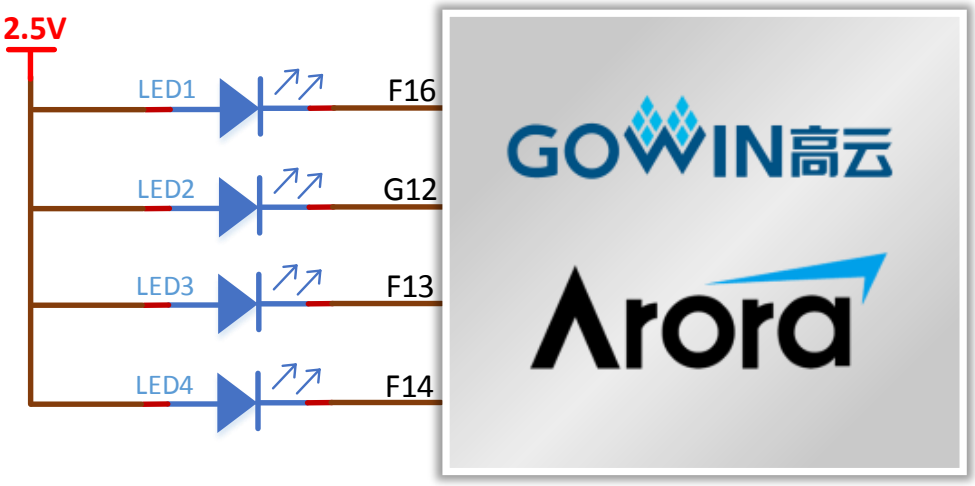
For the V2.0 development board, the BANK0 voltage and BANK1 voltage can be set as 3.3V or 2.5V using J13.

3.10 LED

3.10.1 Introduction

Four blue LEDs are incorporated into the development board and are used to display the required status. If the output signal of the related pins is logic low, LED is on; If logic is high, LED is off. The connection diagram is shown in Figure 3-13.

Figure 3-13 LED Connection Diagram



3.10.2 Pins Distribution

Table 3-11 LED Pins Distribution

Signal Name	FPGA Pin No.	BANK	I/O	Description
LED1	F16	0	2.5V	LED1
LED2	G12	0	2.5V	LED2
LED3	F13	0	2.5V	LED3
LED4	F14	0	2.5V	LED4

Note!

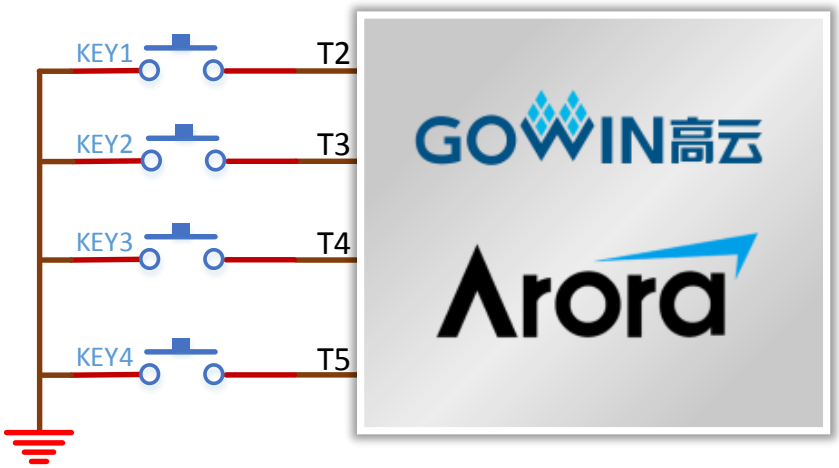
For the V2.0 development board, the BANK0 voltage and BANK1 voltage can be set as 3.3V or 2.5V using J13.

3.11 Key

3.11.1 Introduction

Four key switches are incorporated into the development board. These are used to control input during testing. The connection diagram is shown in Figure 3-14.

Figure 3-14 GPIO Circuit



3.11.2 Pins Distribution

Table 3-12 Key Pins Distribution

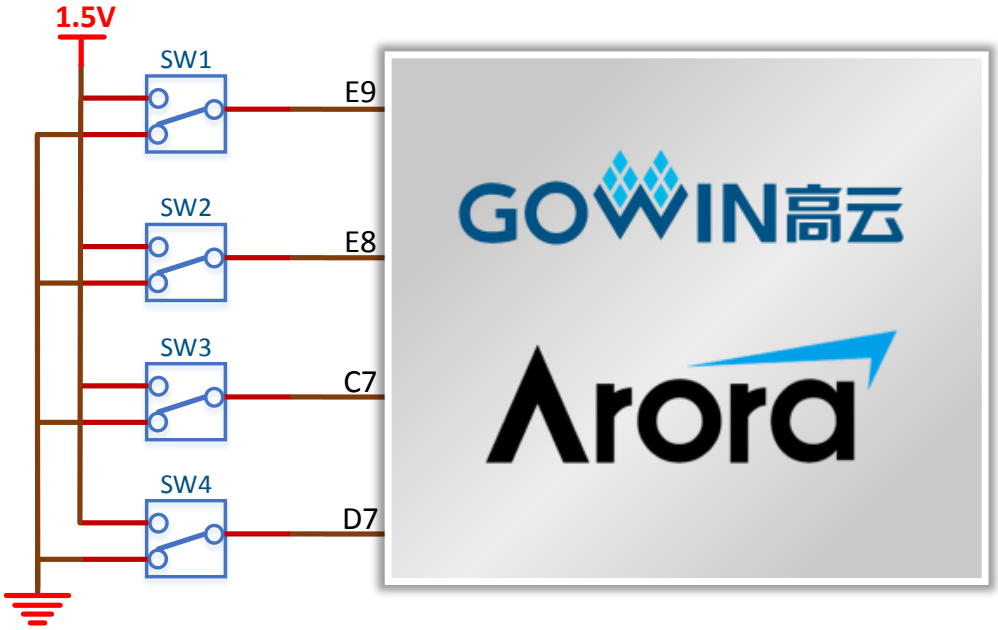
Signal Name	FPGA Pin No.	BANK	I/O	Description
KEY1	T2	4	1.5V	KEY1
KEY2	T3	4	1.5V	KEY2
KEY3	T4	4	1.5V	KEY3
KEY4	T5	4	1.5V	KEY4

3.12 Switch

3.12.1 Introduction

Four slide switches are incorporated into the development board. These are used to control input during testing. The connection diagram is as follows:

Figure 3-15 GPIO Circuit



3.12.2 Pins Distribution

Table 3-13 Pins Distribution of the Switch Module

Signal Name	FPGA Pin No.	BANK	I/O	Description
SW1	E9	6	1.5V	Slide Switch1
SW2	E8	6	1.5V	Slide Switch2
SW3	C7	6	1.5V	Slide Switch3
SW4	D7	6	1.5V	Slide Switch4

4 Gowin YunYuan Software

Please refer to *Gowin Software User Guide* for details.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